Active matrix display device and its driving method.

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Abstract of **EP0554129**

To enhance the display quality by improving the writing characteristic of active matrix display device.
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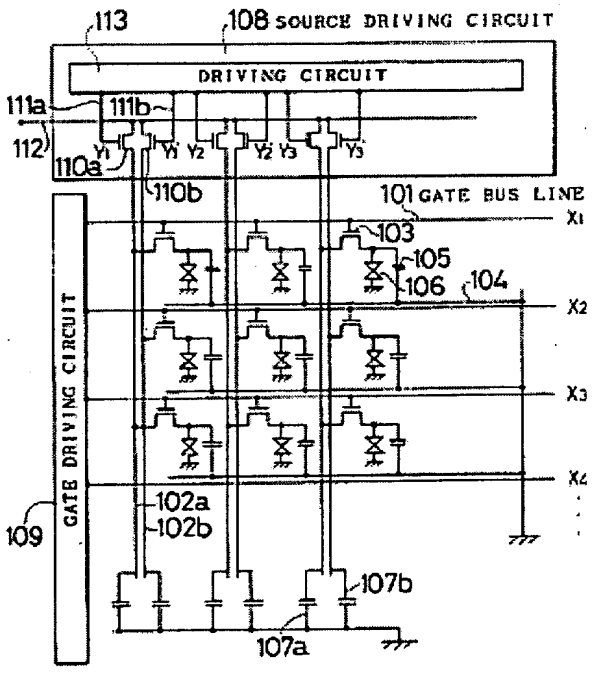
Fig.4



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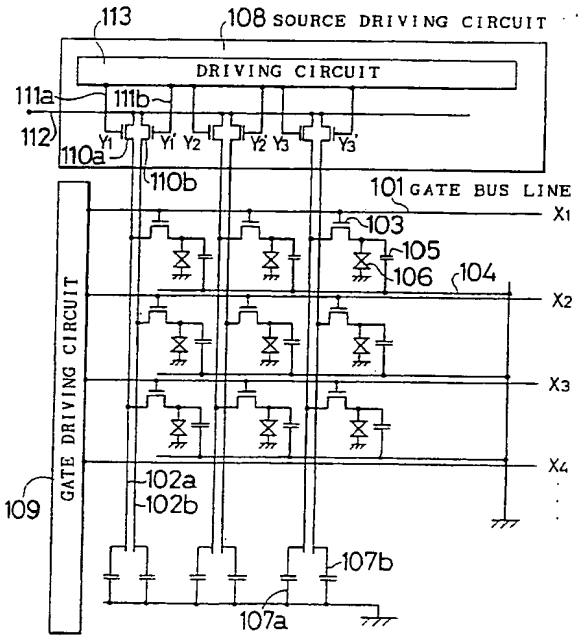
(54) Active matrix display device and its driving method.

(57) To enhance the display quality by improving the writing characteristic of active matrix display device.

A plurality of signal lines (102a, 102b) of video signals are provided for pixels (106) of each column arranged in two-dimensional array, and the driving element (103) of each pixel (106) is designed to be driven by any one of the signal lines (102a, 102b), so that the scanning time of each line (102a, 102b) may be extended longer than one horizontal scanning period.

Fig.4



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BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an active matrix display device used in a liquid crystal display device and the like, and its driving method.

2. Description of the Related Art

Fig. 1 shows an example of construction of an active matrix liquid crystal display device having pixels of n rows and m columns in the prior art. A basic constitution of such prior art is disclosed, for example, in pages 152-154 of JAPAN DISPLAY '89. In the prior art shown in Fig. 1, additional capacitances are connected parallel to the pixel (electrically equivalent to capacitance). In the drawing, numeral 603 is a switching element composed of a thin film transistor (hereinafter called TFT), which is turned on or off by a gate signal sent from a gate driving circuit 609 through a gate bus line 601. Numeral 608 denotes a source driving circuit, which is composed of analog switches 610 for sampling video signals sent from a video signal line 612 and writing into source bus line with capacitances 607, and a shift register 613 for sending the sampling control signal to gate electrode 611 of the analog switch.

A video signal supplied to the source bus line 602 through the source driving circuit 608 is written into a pixel 606, which is equivalent to a capacitance being composed of a liquid crystal held between a pixel electrode disposed on each pixel and a counter electrode on a counter substrate, and into an additional capacitance 605 for compensating the capacitance of the pixel being connected parallel to this pixel 606 when the potential of the gate pulse line 601 becomes high and the pixel TFT 603 is turned on.

One terminal of this additional capacitance 605 is connected to the pixel electrode, and the other is connected to an additional grounded capacitance line 604. The written signal is held in the OFF state of the TFT 603, but by installing the additional capacitance 605, the holding characteristic of this signal may be improved, or the fluctuations of characteristics due to anisotropy of dielectric constant of the liquid crystal may be alleviated.

Fig. 2 and Fig. 3 show examples of driving waveforms of conventional active matrix liquid crystal display device. Fig. 2 depicts signal waveforms delivered from the gate driving circuit 609 into individual gate bus lines X_1, X_2---X_n during one field. The signal "H" corresponds to the ON state of the pixel TFT 603, and "L" to the OFF state. Thus, in the sequence of the gate bus lines X_1, X_2---X_n, the signal "H" is issued, and the pulse width of the output is nearly equal to the horizontal scanning time (known as "1H"). In this period of "1H", for on/off control of the analog switch 610 in the source driving circuit 608, control signals having the waveform as shown in Fig. 3 are applied to the gate electrode of each analog switch 610.

The diagram shows the waveform when the i-th and i+1-th gate bus lines X_i, X_{i+1} are ON, as is similar in other cases. In this example, incidentally, the timing of the change of potential of the i-th gate bus line X_i from "H" to "L" coincides with the timing of change of the potential of the (i+1)-th gate bus line X_{i+1} from "L" to "H". In this period of 1H, the m analog switches 610 are sequentially turned on, and the video signals are written into the source bus lines 602.

A finite time t1 must be provided from the moment of the previous stage gate bus line X_{i-1} becoming L until the first analog switch 610 is turned on by the control signal Y_1. This is because the resistance of the gate bus line 601 is finite and the potential change is delayed. That is, if a video signal is written in the source bus line 602 by turning on the analog switch 610 by control signal Y_1 before the previous stage gate bus line X_{i-1} becomes sufficiently "L", since the resistance of the pixel TFT 603 connected to the previous stage gate bus line X_{i-1} is not sufficiently increased, the signal written in the previous stage pixel 606 may be disturbed by the video signal corresponding to the pixel 606 of this stage.

As a result, the display of the previous stage pixel is a mixture of the video signal for the previous stage and the video signal for the next stage, and the resolution is lowered. Therefore, the time t1 should be set sufficiently long in order to decrease the effect of delay time of the gate bus line 601. Likewise, a finite time t2 must be provided from the moment of turning on the final analog switch 610 by control signal Y_m until the potential of the gate bus line 601 is lowered to "L". This is because a finite time is required for writing signals into the pixel 606 and additional capacitance 605 through the pixel TFT 603, and discharging the written charge through the additional capacitance wiring 604, and the video signal cannot be sufficiently written into the pixel 606 unless a sufficiently long time is taken.

It was thus a feature of the conventional active matrix liquid crystal display device that only one source bus line 602 was connected to each pixel 606. In the driving method of the conventional active matrix display device, it was a feature that the ON time of each gate bus line 601 did not exceed the horizontal scanning time.

In the conventional active matrix type liquid crystal display device, the greater the number of pixels, the higher becomes the resolution, and a favorable display quality may be obtained. However, as the number of pixels increases, several technical problems occur. For example, delays of the gate bus line and additional capacitance common line are notable. The line resistance and additional capacitance are both proportional to the number of pixels in the hori-

zontal direction. Therefore, the time constant of delay of these lines is nearly proportional to the square of the number of pixels in the horizontal direction. Hence, as the number of pixels increases, the line delay increases noticeably. Accordingly, the times t1, t2 must be extended.

In the display device having a great number of pixels, however, the horizontal scanning time becomes shorter. As a result, sufficiently long duration cannot be taken for times t1, t2 in order to decrease the effect of delay, which results in an increase of the effect of delay. When such effect of line delay increases, deterioration of display quality or the like may occur at one end of the screen. It is hitherto very difficult to improve the resolution without sacrificing the display quality. Besides, along with the increase of the number of pixels, the signal writing time for one pixel becomes shorter in proportion. Hence, it is also a problem that a faster writing speed of signal is required.

The present inventors have previously disclosed some improved inventions in the Japanese Patent Publications No. 163529/1991 and No. 163530/1991, with the purpose of reducing the effect of signal delay on display quality. In these inventions, by lowering the resistance of the additional capacitance line, the signal writing speed is enhanced.

It is similarly an object of the present invention to reduce the effect of signal delay on display quality. In the invention, however, this object is achieved by completely different means for substantially extending the writing time.

To achieve the above object, the invention presents an active matrix display device comprising pixels in two-dimensional arrangement, and having each pixel provided with a driving element for driving the pixel, wherein a plurality of signal lines for feeding signals to driving elements of pixels in each column are formed at each column, that the driving element of each pixel may be driven by any one of the signal lines.

In the invention, the pixel driving element of each row is arranged to be driven by a signal from a signal line different from the driving element of the adjacent row.

Also in the invention, the pixel driving element in each row comprises means for successively generating signals and for supplying the signals to the pixel driving element of each row to make active during the scanning time which is a product of one horizontal scanning time and a number of signal lines formed in each column.

In the invention, the pixel driving elements are constructed as thin film transistors. In the invention, the signal provided for each column driving element is kept by capacity of signal line for the moment.

The invention also presents a driving method of an active matrix display device for driving a matrix display device, which is composed of pixels in two-dimensional arrangement, and driving elements disposed at each pixel, for driving by means of selection signal for each column and video signal for each row, wherein

a plurality of signal lines for feeding signals to driving elements of pixels in each column are formed, and the driving element of each pixel is driven by any one of the signal lines, so that the scanning time of the selection signal, when the driving element for driving pixels of each row is active, may be a product of one horizontal scanning time and a number of signal lines formed in each column.

In the invention, the driving elements of pixels of each column are constructed so that the driving element of pixels of each adjacent row may be driven by a video signal from a different signal line.

Also in the invention, the driving elements of pixels of each row are provided with a selection signal sequentially for making active only during the scanning time, while deviating the section signal by a predetermined time.

In the invention, moreover, the driving elements of pixels of each row are provided with a video signal through one of the signal lines formed in a plurality at each column, after each row is made active by a selection signal and before the next row is made active by a selection signal.

According to the above constitution, if ON signals are simultaneously sent to a plurality of adjacent gate bus lines, video signals to be written into adjacent pixels across gate bus lines will not be mixed mutually. Therefore, the output width of the ON signal sent out to each gate bus line may be set longer than the time assigned for one gate bus line. As a result, the time for decreasing the delay effect of signal line may be extended, and the effect of line delay may be decreased if the number of pixels is increased, so that the display quality may be enhanced.

The invention is thus constructed so that the sum t1+t2+t3 can be extended to 2H and so forth, where the time t1 is from the moment when the gate bus line becomes high until reading of video signal to the first source bus line begins, the time t2 is from the moment when the video signal is read out to the final source bus line until the output of the gate bus line falls, and the time t3 is required to read out the video signal for pixel array of one row. In the conventional driving wave form, the sum is one horizontal time (1H). Therefore, the duration of t1, t2, t3 can be extended, and the effect of the line delay is lessened accordingly, so it is possible to present a display device excellent in writing characteristic of the pixel transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

Other and further objects, features, and advantages of the invention will be more explicit from the

following detailed description taken with reference to the drawings wherein:

Fig. 1 is a structural diagram of a prior art.

Fig. 2 is an operation explanatory diagram of Fig. 1.

Fig. 3 is an operation explanatory diagram of Fig. 1.

Fig. 4 is a structural diagram of an embodiment of the invention.

Fig. 5 is an operation explanatory diagram of Fig. 4.

Fig. 6 is an operation explanatory diagram of Fig. 4.

Fig. 7 is a plan structural diagram showing a pratical constitution of essential part of Fig. 4. and

Fig. 8 is a sectional view from line A-A' of Fig. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Now referring to the drawing, preferred embodiments of the invention are described below.

Fig. 4 shows an example of circuit construction of an active matrix display device according to the invention. Fig. 7 further shows an example of layout for TFT array part of this active matrix display device. Herein, numeral 101 denotes a gate bus line, which is connected to a gate electrode 103G of a pixel TFT 103 composed of two TFTs connected in series. Numeral 109 is a gate driving circuit, which sends out an on/off signal for the pixel TFT 103 to the gate bus line 101.

Numeral 108 is a source driving circuit, which is composed of analog switches 110a, 110b interposed between a video signal line 112 and source bus lines 102a, 102b, and a driving circuit 113 for sending nut the on/off control signals of the analog switches 110a, 110b to the gate electrodes of the analog switches 110a, 110b. The video signal is sent out to the source bus lines 102a, 102b through the source driving circuit 108 at adequate timing, written into capacitances 107a, 107b of the source bus lines, and further written into, a specific pixel through the pixel TFT 103 in ON state.

The written video signal is written, in the OFF state of the pixel TFT 103, into a pixel 106 which is equivalent to a capacitance formed with a liquid crystal held between a pixel electrode 116 and a counter electrode and into an additional capacitance 105 connected parallel to the pixel. One electrode 105x of the additional capacitance 105 is connected to an additional capacitance common line 104, and is grounded. In one pixel array, a pair of source bus lines 102a, 102b are disposed, which are connected alternately on every other row to source electrodes 103Sa, 103Sb of the pixel TFT 103 through contact holes 114a, 114b, respectively as shown in Fig. 7.

A drain electrodes 103D of the pixel TFT 103 is connected to the other electrode 105y of the additional capacitance 105 and to a pixel electrode 116 through contact holes 115a, 115b as shown in Fig. 7.

A sectional structure along line A-A' of Fig. 7 is shown in Fig. 8. On a transparent insulating substrate 121, a polycrystalline silicon film 122 serving as a channel portion 103c of the TFT 103 and the other electrode 105y of the additional capacitance 105, a gate insulation film 123, and a polycrystalline silicon film 124 doped with impurities serving as the gate electrode 103G of the TFT 103 and the one electrode 105x of the additional capacitance 105 are formed in this order. In specified parts of the polycrystalline silicon film, impurities are doped by ion implantation method. An insulating film 125 is formed in the upper part of the polycrystalline silicon film 124, and the contact hole 115a is opened, and the pixel electrode 116 is formed by wiring such as source bus line of low resistance metal like as Aluminium (Aℓ), and transparent conductive thin film like as ITO.

Fig. 5 and Fig. 6 show driving waveforms in the embodiment. Fig. 5 shows the signal waveform in one vertical scanning period (one field) sent out to gate bus lines X_1 through X_n. When the potential of each gate bus lines X_1 to X_n becomes "H" level, the transistors, the gate electrodes of which the gate bus lines X_1 to X_n are connected to, are turned on at the same time. In each gate bus line, the ON signal is sent out for the double duration of one horizontal scanning period (1H). The gate bus lines X_1 to X_n send out signals at the timing deviated by the time of 1H sequentially as shown in Fig. 5, and the output pulses of adjacent gate bus lines are overlapped by the duration of 1H.

Fig. 6 shows the detail about driving waveform in two horizontal scanning periods (2H). In the drawing, X_i and X_{i+1} are driving waveforms of the i-th and (i+1)-th gate bus lines respectively. Besides, Y_1, Y'_1, Y_2, Y'_2 to Y_m, Y'_m are gate signals to be fed into gate electrodes of the analog switches 110a, b respectively, and when the gate signal becomes "H", the corresponding analog switches 110a, b are turned on, and the video signal sent from the video signal line 112 is written into specific source bus lines 102a, b, and the video signal is further written into the specific pixel through the pixel TFT 103 in ON state.

In this embodiment, first the gate bus line X_i becomes "H", and t1 time later the gate signal Y_1 of the analog switch 110a becomes "H", and when the video signal is written in the corresponding source bus line, "H" is sent out on the previous stage gate bus line X_{i-1}. However, since the source bus line corresponding to the gate signal Y_1 is not connected to the TFT connected to the gate bus line X_{i-1}, mixture of video signal does not occur because of the difference in the pulse width of the gate bus line.

In the embodiment, by installing two source bus lines for one pixel column, the pulse width of each gate bus line is set twice as long as one horizontal

scanning period for driving in the state free from mixture of video signals, but the effect of the embodiment is not limited to this case alone, and when more source bus lines are provided, the output pulse width of the gate bus line may be set to a multiple of the number of source bus lines per pixel column in one horizontal scanning period.

Further in the embodiment, the writing time of video signal may be extended. By once converting the incoming video signal into a digital signal, storing the digital signal into a memory, and converting the stored signal into an analog signal again at specific timing, the writing time of video signal for pixel may be extended. As a result, the required characteristic of the analog switch may be alleviated, and the writing characteristic of the video signal is further enhanced, so that the display quality may be more improved.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come within the meaning and the range of equivalency of the claims are therefore intended to be embraced therein.

Claims

1. An active matrix display device having pixels (106) arranged two-dimensionally and driving elements (103) provided for each pixel (106) to drive the pixel (106), wherein a plurality of signal lines (102a, 102b) for feeding signals to driving elements (106) provided for column pixels (106) are formed in each column, so that the driving element (103) of each pixel (106) may be driven by any one of the signal lines (102a, 102b).

2. An active matrix display device as in claim 1 , wherein driving elements (103) of each row are arranged to be driven by a signal line (102a, 102b) different from signal lines (102a, 102b) for driving element (103) of the adjacent row.

3. An active matrix display device as in claim 2, further comprising means (109) for successively generating signals and for supplying the signals to the pixel driving element (103) of each row to make active during the scanning time which is a product of one horizontal scanning time and a number of signal lines formed in each column.

4. An active matrix display device as in any one of claims 1 to 3, wherein the pixel driving element (103) being a thin film transistor.

5. An active matrix display device as in any one of claims 1 to 3, wherein the signal provided for each column driving element (103) being kept by capacitances (107a, 107b) of each signal line (102a, 102b) for the moment.

6. A driving method of an active matrix display device, which is composed of pixels (106) in two-dimensional arrangement and driving elements (103) disposed at each pixel (106), for driving by means of selection signal for each column and video signal for each row, wherein

forming a plurality of signal lines (102a, 102b) for feeding signals to the driving elements (103) of pixels (106) in each column are formed, and driving the driving element (103) of each pixel (106) by any one of the signal lines (102a, 102b), so that the scanning time of the selection signal being a product of one horizontal scanning time and a number of signal lines (102a, 102b) formed in each column when the driving element (103) for driving pixels (106) of each row being active.

7. A driving method of an active matrix display device as in claim 6, wherein

driving the driving element (103) of pixels (106) of each adjacent row by a video signal from a different signal line (102a, 102b).

8. A driving method of an active matrix display device as in claim 7, wherein providing the driving elements (103) of pixels (106) of each row with a selection signal sequentially for making active only during the scanning time, while deviating the selection signal by a predetermined time.

9. A driving method of an active matrix display device as in claim 8, wherein providing the driving elements (103) of pixels (106) of each row with a video signal through one of the signal lines (102a, 102b) formed in a plurality at each column, after each row being made active by a selection signal and before the next row being made active by a selection signal.

10. A driving method of an active matrix display device as in any one of claims 6 to 9, wherein keeping the signal provided for each column driving element (103) by capacitances (107a, 107b) of each signal line (102a, 102b) for the moment.

Fig.1

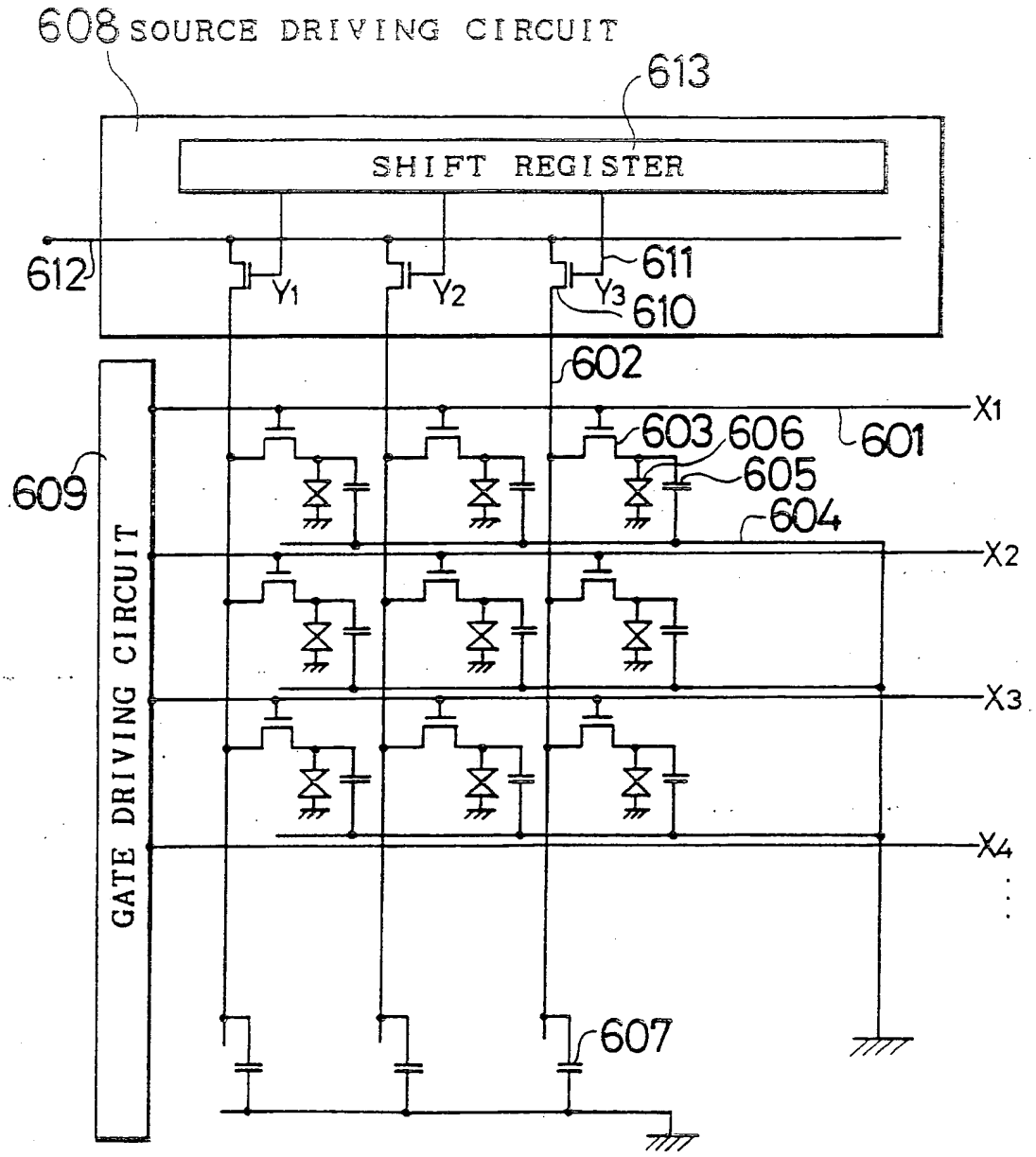

608 SOURCE DRIVING CIRCUIT
613
SHIFT REGISTER
612
Y1
Y2
Y3
611
610
602
601
603
606
605
604
609
GATE DRIVING CIRCUIT
X1
X2
X3
X4
607

Fig. 2

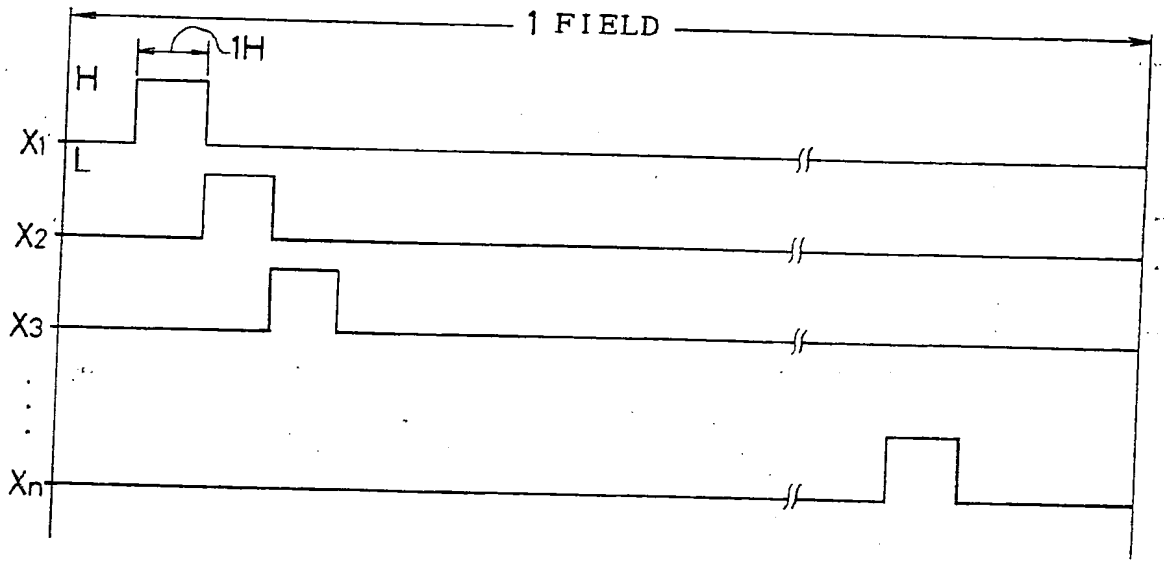


Fig. 3

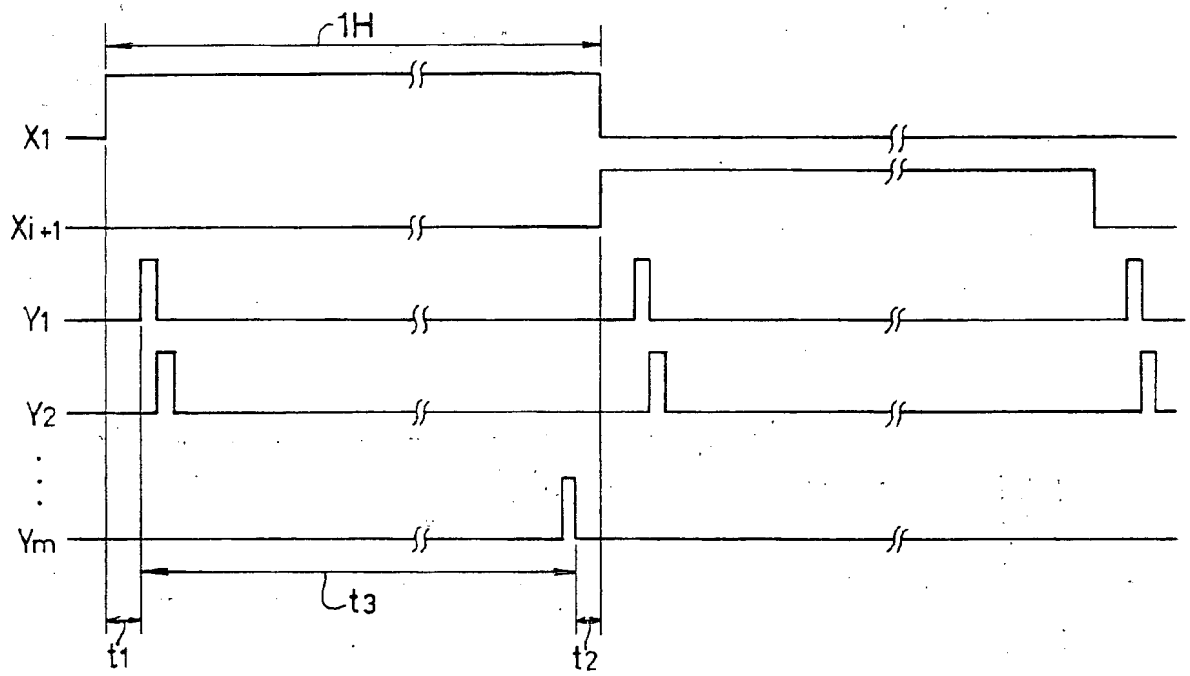


Fig. 4

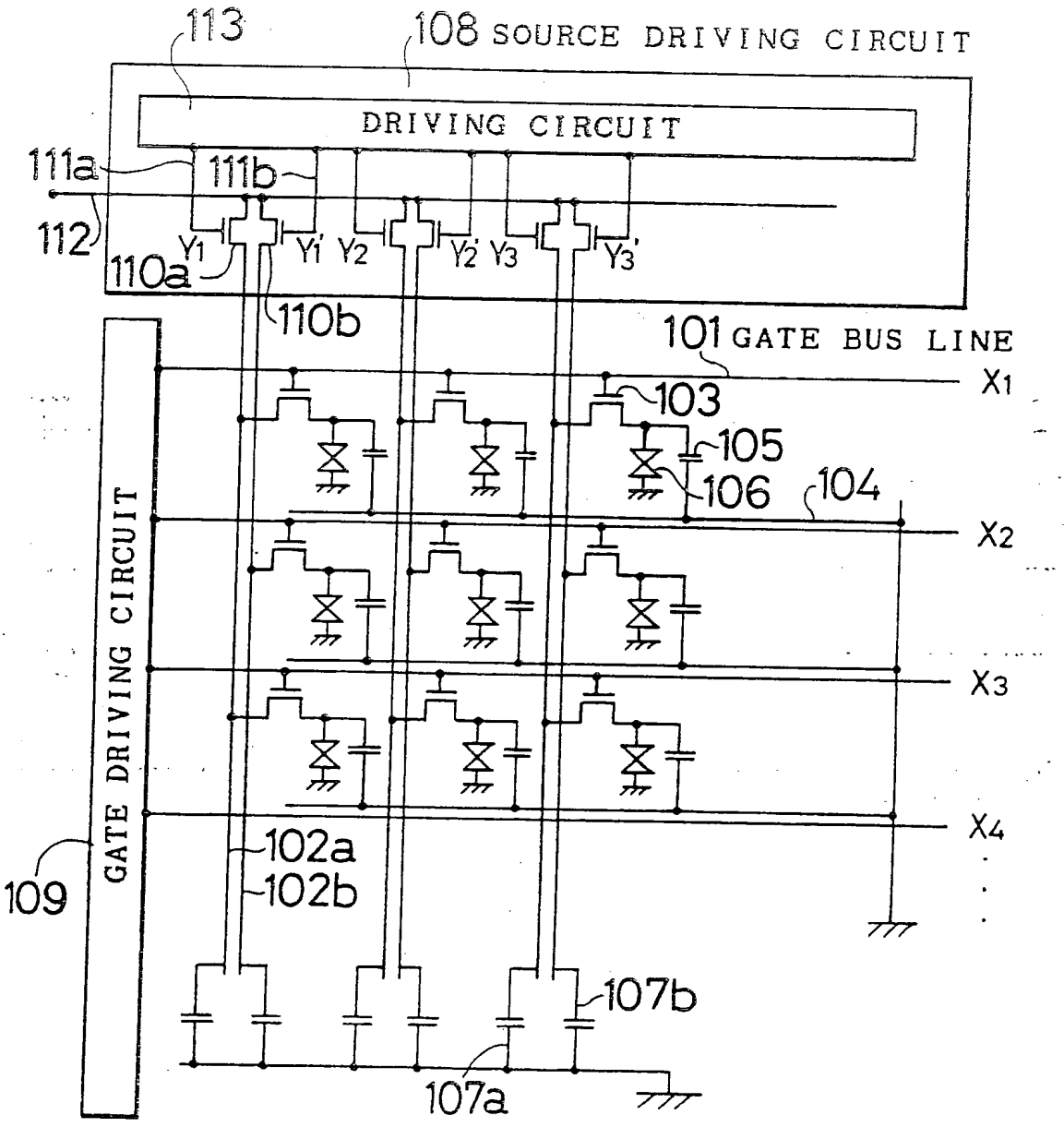


Fig. 5

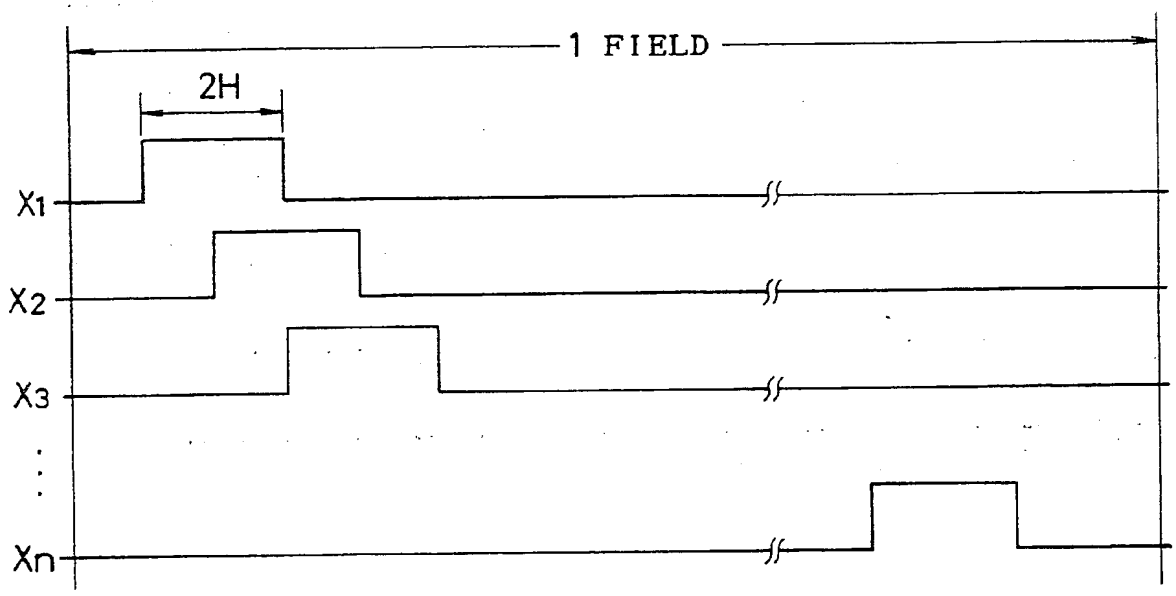


Fig. 6

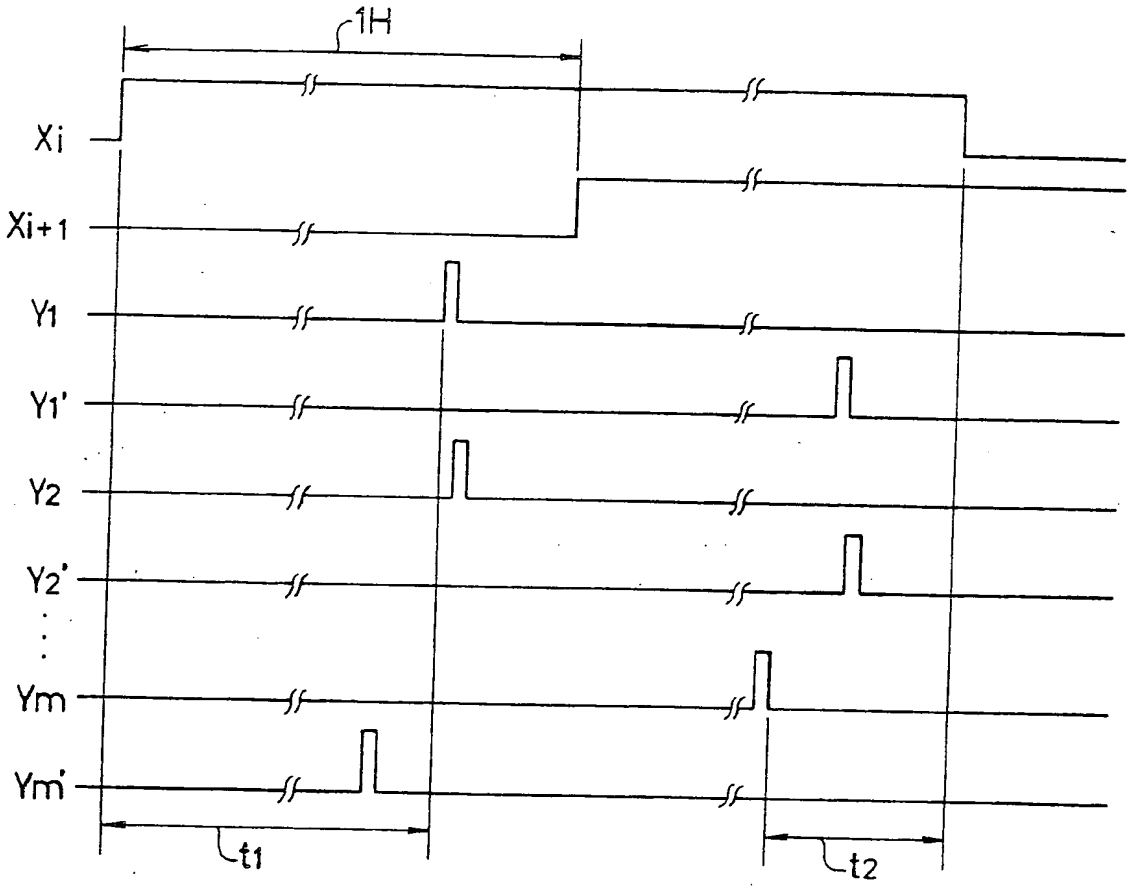
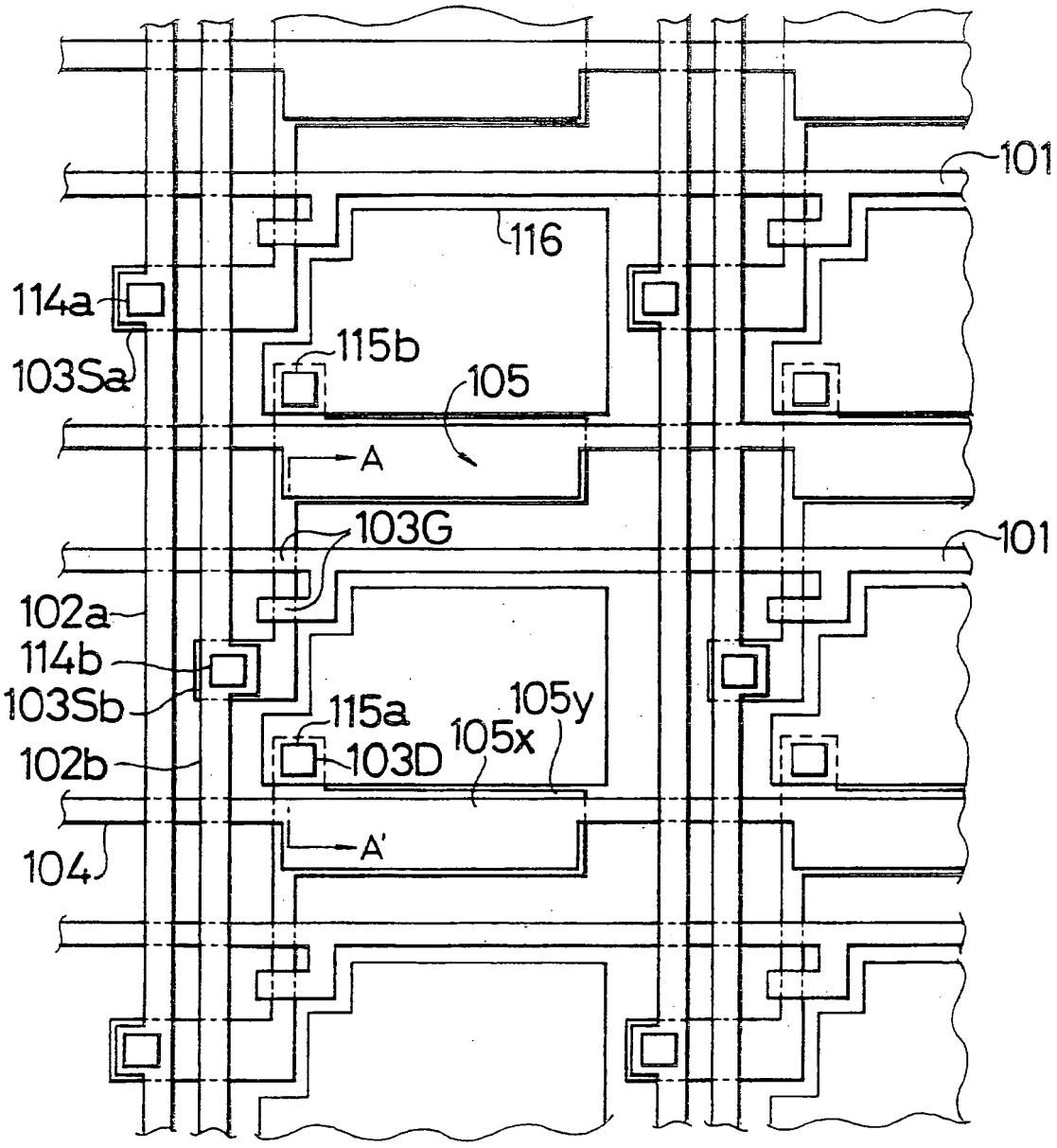


Fig. 7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114a
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105
A
103G
101
102a
114b
103Sb
115a
105y
105x
102b
103D
A'
104

Fig. 8